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TITLE OF THE INVENTION

FACILITATING ERROR DETECTION FOR CONTENT ADDRESSABLE MEMORY

BACKGROUND OF THE INVENTION

[0001] CAM is memory that provides an address on its output bus when read. The address corresponds to the storage location of data provided at its input bus. The data (e.g., a data word) is known as a comparand or a key. Addresses in CAM are searched in parallel and produce the address storing associated data. The associated data is typically stored in separate, discrete memory in a storage location specified by the result of the CAM search. In this manner, CAM search functionality enables extremely quick searches of content.

[0002] CAM is used in ATM switches for connection identifier compression, whereby a 28-bit VPI/VCI (virtual path identifier/virtual circuit identifier) connection identifier is translated into an 18-bit connection identifier. This translation is necessary when a linecard in the switch can only support 256K connections (18-bit identifier) as compared to the 256M connections supported by the 28-bit VPI/VCI connection identifier specified by the ATM standard.

[0003] Conventional implementations of CAM are limited in that they do not offer adequate error detection to provide indication of when an error occurs on the input bus, storage array or output bus of the CAM. Accordingly, conventional implementations of CAM are limited in their ability to facilitate data retrieval in a manner that is required by a carrier-class ATM switch. Therefore, method and equipment adapted for providing error detection in conventional implementations of CAM would be useful.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

[0004] The present invention may be better understood, and its features made apparent to those skilled in the art by referencing the accompanying drawings.

[0005] FIG. 1 depicts a method for facilitating error detection for CAM in accordance with an embodiment of the disclosures made herein.

[0006] FIG. 2 depicts an apparatus adapted for facilitating error detection for CAM in accordance with an embodiment of the disclosures made herein.

[0007] The use of the same reference symbols in different drawings indicates similar or identical items.

DETAILED DESCRIPTION OF THE INVENTION

[0008] The disclosures made herein relate to methods and apparatuses adapted for facilitating data error detection associated with conventional Content Addressable Memory (CAM) modules. Such methods and apparatuses are referred to hereinafter as disclosed CAM error detection methods and disclosed CAM error detection apparatuses, respectively, which provide corresponding disclosed CAM error detection functionality. Conventional CAM modules are defined herein to include off-the-shelf CAM modules that are not specially configured or specifically configured for facilitating error detection of a CAM module storage array, a CAM module input bus and/or a CAM module output bus.

[0009] Disclosed CAM error detection methods and disclosed CAM error detection apparatuses provide CAM error detection functionality for the CAM module storage array, the CAM module input bus and the CAM module output bus. Providing error detection on input data and output data of conventional CAM modules is more cost-effective than designing and implementing non-conventional CAM modules, particularly when means for providing such disclosed CAM error detection functionality is less costly than implementing non-conventional CAM modules.

[0010] Unlike conventional implementations of CAM error detection functionality, disclosed CAM error detection functionality enables conventional CAM modules to be used for Connection Identifier (CI) compression in a manner that meets requirements of carrier-class ATM switches. Because disclosed CAM error detection functionality enables carrier-class ATM switches to be manufactured with conventional CAM modules, which are cost-effective, switches incorporating disclosed methods and/or disclosed apparatuses are advantageous with respect to cost and performance of conventional switches. Hence, the competitiveness of ATM switches incorporating disclosed CAM error detection functionality is improved.

[0011] It will be appreciated that application of disclosed CAM error detection functionality is not limited to ATM switches. A skilled person will find that disclosed

CAM error detection functionality is useful in numerous applications where reliable use of CAM storage retrieval of information is desirable and/or necessary.

[0012] Turning now to specific drawing figures, FIG. 1 depicts a method 100 adapted for facilitating data error detection for CAM modules in accordance with an embodiment of the disclosures made herein. An operation 102 is performed for generating a parity word based on a key (i.e., key-based parity word). The key is received from a requesting system entity. The parity word comprises one or more bits. The value of the one or more bits is a function of the key. The parity word may be obtained using known error detection techniques (e.g., cyclical redundancy check, bit interleaved parity generating, etc.) A 28-bit VPI/VCI word is an example of a basis for the key in ATM applications. The key and the key-based parity word jointly define a comparand.

[0013] After generating the key-based parity word, an operation 104 is performed for searching storage of a CAM module for an address containing data corresponding to the comparand after the comparand is provided to the CAM module. If a data error (e.g., a bit error) has occurred anywhere in the comparand, an address containing data corresponding to the comparand will not be found in the storage of the CAM module. In response to a failure in making a comparand match in the storage of the CAM module at an operation 105, an operation 106 is performed for issuing an input error indication. The input error indication means that a data error has occurred somewhere in the comparand, or that the original key was not found in the CAM.

[0014] In response to a comparand match being made in the storage of the CAM module at the operation 105, an operation 108 is performed for accessing a predetermined protection word that corresponds to the address containing data corresponding to the comparand. Searching memory including a plurality of predetermined protection words and finding the predetermined protection word is an example of accessing the predetermined protection word. In response to a comparand match being made in the storage of the CAM module or prior to searching the storage of the CAM module for the address containing data corresponding to the comparand, an operation 110 is performed for generating a protection word based on the key (i.e., key-based protection word).

[0015] After generating the key-based protection word and after the predetermined protection word is accessed, an operation 112 is performed for comparing the predetermined protection word with the key-based protection word. In response to determining that the predetermined protection word is different than the key-based protection word at an operation 113, an operation 114 is performed for facilitating (e.g., issuing) an output error indication. The output error indication means that the address from the CAM has not accessed a matching protection word in the memory and, hence, the address is corrupt. In response to determining that the predetermined protection word matches the key-based protection word at the operation 113, an operation 116 is performed for providing the address to the requesting system entity.

[0016] An input error detection process for detecting errors on an input bus on a CAM module comprises generating the key-based parity word, searching storage of the CAM module and issuing the input error indication. An output error detection process for detecting errors on an output bus of a CAM module comprises accessing the predetermined protection word, generating the protection word based on the key (i.e., key-based protection word), comparing the predetermined protection word with the key-based protection word and issuing the output error indication.

[0017] FIG. 2 depicts an embodiment of an apparatus 200 capable of carrying out the method 100 of FIG. 1. An ATM switch is an example of the apparatus 200. Carrying out the method 100 via the apparatus 200 enables CAM error detection functionality in accordance with an embodiment of the disclosures made herein.

[0018] The apparatus 200 includes a Connection Manager (CM) 202 connected to a CAM module 204. The CM 202 includes a parity word generator 206, a protection word generator 208, memory 210 and a comparator 212. The CAM module 204 includes a storage array 214. The parity word generator 206 is connected to the storage array 214. The protection word generator 208 and the memory 210 are connected to inputs of the comparator 212. The memory 210 is connected between the output of the storage array 214 and one of the inputs of the comparator 212.

[0019] The parity word generator 206 is adapted for generating a parity word upon being provided a key 216 (i.e., a key-based parity word 218). The key-based parity word 218 and the key 216 jointly define a comparand, which is provided to the storage array 214 of the CAM module 204. The storage array 214 of the CAM module 204 is searched in an attempt to access an address 220 containing data that corresponds to the comparand.

[0020] An appropriate portion of the CAM module 204 (not specifically shown) provides an error notification 222 to the CM 202 if a data error (e.g., a bit error) has occurred in the comparand. A data error in the comparand prevents the address 220 containing data that corresponds to the comparand from being accessed in the storage array 214 of the CAM module 204. The error notification 222 is provided to the CM 202 for enabling an input error indication 224 to be issued. An input error detection module comprises the parity word generator 206 and means (not specifically shown) of the CM 202 adapted for issuing the input error indication 224.

[0021] The protection word generator 208 generates a protection word from the key 216 (i.e., a key-based protection word 226). A device capable of generating a cyclical redundancy code or a bit interleaved parity word is an example of the protection word generator 208. A plurality of predetermined protection words (e.g., 4 bit protection words) is stored in the memory 210 of the CM 202. When the address 220 containing data that corresponds to the comparand is accessed in the storage array 214 of the CAM module 204, the memory 210 of the CM 202 is searched for accessing a predetermined protection word 228 corresponding to the address 220 assessed from the storage array 214 of the CAM module 204.

[0022] The comparator 212 compares the key-based protection word 226 with the predetermined protection word 228. When the key-based protection word 226 is different than predetermined protection word 228 (i.e., when inputs of the comparator 208 are not equal), the address 220 from the CAM module 204 has not accessed a matching predetermined protection word in the memory 210. Hence, the address 220 is corrupt and the comparator 212 facilitates issuance of an output error indication 230.

[0023] An input error detection module capable of detecting errors on an input bus on a CAM module comprises the parity word generator 206 and means (not shown) of the CM 202 adapted for issuing the input error indication 224. An output error detection module capable of detecting errors on an output bus on a CAM module comprises the protection word generator 208, the memory 210 and the comparator 212.

[0024] A data processor program in accordance with an embodiment of the disclosures made herein controls at least a portion of the operations associated with facilitating disclosed CAM error detection functionality. Such a data processor program is processible by a data processor of an apparatus in accordance with an embodiment of the disclosures made herein for carrying out operations of a method in accordance with an embodiment of the disclosures made herein. Furthermore, such a data processor program may be resident on one or more data processing modules (e.g. a card including the data processor) or may be accessible by the data processor from an apparatus such as a diskette, a compact disk, a network storage device, a component of the network system or other suitable apparatus. The term data processor program refers to computer software, data processor algorithms or any other type of/sets of instruction code capable of controlling operations associated with a data processor.

[0025] A microprocessor, an application specific integrated circuit (ASIC), a field-programmable gate array (FPGA) and other types of programmable logic devices (PLDs) are examples of data processors capable of facilitating disclosed CAM error detection functionality. For example, it is contemplated herein that a FPGA may be used to generate parity and protection words, with appropriate software being used to configure the FPGA appropriately and to report any detected errors.

[0026] A data processor program accessible from an apparatus by a data processor is defined herein as a data processor program product. A read-only memory (ROM), a programmable read-only memory (PROM), an erasable programmable read-only memory (EPROM), an electrically erasable programmable read-only memory (EEPROM), an electrically alterable programmable read-only memory (EAPROM), a flash memory, other non-volatile memory (NVM), a compact disk (CD/CDR/CDRW), or a digital video

disk (DVD/DVDR/DVDRW) having a data processor program adapted for carrying out disclosed CAM error detection functionality are examples of a data processor program product.

[0027] In the preceding detailed description, reference has been made to the accompanying drawings that form a part hereof, and in which are shown by way of illustration specific embodiments in which the invention may be practiced. These embodiments have been described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be utilized and that logical, mechanical, chemical and electrical changes may be made without departing from the spirit or scope of the invention. To avoid detail not necessary to enable those skilled in the art to practice the invention, the description omits certain information known to those of skill in the art. The preceding detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims.